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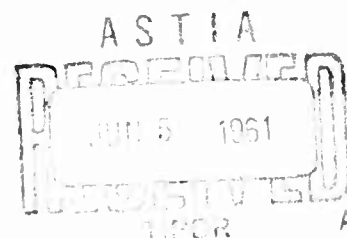
**THE 2D-BINARY DIVIDER--  
ITS HISTORY, PERFORMANCE, AND INTERCONNECTION**

**Norman J. Doctor**

**10 April 1961**

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**FOR THE COMMANDER:**  
**Approved by**

  
**Philip J. Franklin**  
**Chief, Laboratory 900**



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## ABSTRACT

Two hundred 2D-binary dividers were purchased from the Sprague Electric Co. and subsequently evaluated and interconnected. A failure rate of about 10 percent/1000 hr for these initial binary divider wafers indicated that they are not, as yet, reliable items. The primary weakness in the 2D units is at the point of connection of the semiconductor devices to the circuit substrate via a conductive adhesive.

Limited success has been experienced with deposited metal and welded interconnection techniques and the assignment of these problems to a group with strong mechanical engineering background is recommended. Jigs, fixtures and techniques employed to date are detailed.

### 1. INTRODUCTION

In November 1957 the 2D concept for fabricating extremely tiny electronic assemblies was developed and its feasibility established (ref 1). The 2D packaging concept involves the use of substrates on which conductors, resistors, and often capacitors are printed while uncased semiconductor devices are inserted, and electrically and mechanically attached. In the months that followed the initial development, small quantities of two types of digital circuits, binary dividers, and NOR's (ref 2) were fabricated, cursorily evaluated, and employed in certain interconnected configurations.

Because of the limited staff available at the Laboratories for the production of sufficient units to allow a more thorough investigation of the behavior of these 2D assemblies, contractual assistance was obtained. A purchase order was made with the Sprague Electric Co. for 200 2D-NOR circuits, and the first delivery was made on 6 January 1959. The NOR circuit, a schematic diagram of which is shown in figure 1, was chosen for these reasons:

- (1) It is a rather elementary circuit in that it contains only one transistor and four resistors.
- (2) It is a circuit that allows direct measurement of the  $\beta$  and  $I_{CO}$  of the transistor via the circuit leads.
- (3) It is a universal building block for logic-type circuitry and could be employed in building subassemblies requiring exclusively that 2D circuit wafer type.

Preliminary results obtained from the first 25 2D-NOR's were reported by Prugh (ref 3). His conclusions on nonhermetically sealed units showed that  $\beta$ 's increased upon room temperature storage of five units and decreased when two units were stored at 75°C. He also noted a relatively small decrease in  $\beta$  and no catastrophic failures on temperature cycling six units. It was also cited that potting decreased  $\beta$ 's of nine units by a factor between 1.5 to 1 and 2 to 1.

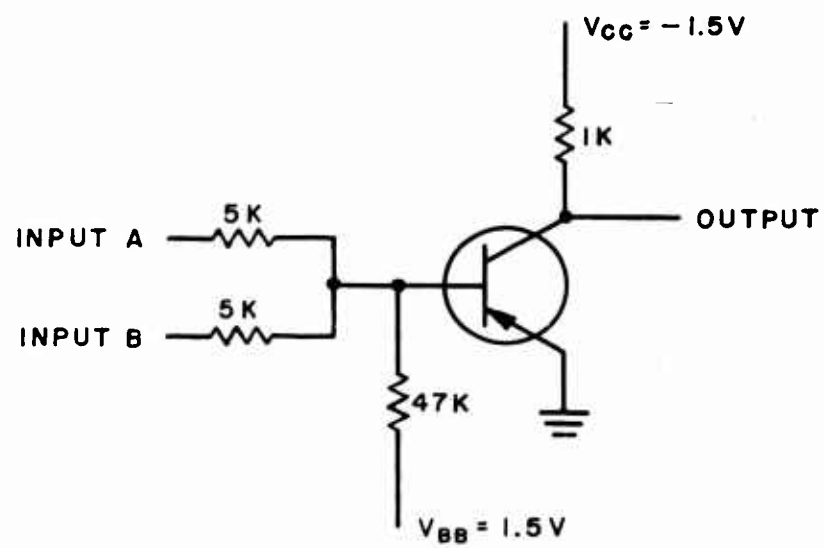


Figure 1. Schematic diagram of NOR circuit.

As more units were delivered, attempts were made to form subassemblies by deposited metal interconnection techniques (ref 4). Groups of five or six NOR's were stacked, potted, machined, and interconnected with deposited metal. Most subassemblies made in this manner failed to operate and further investigation showed that at least one NOR in each potted subassembly was no longer operating. Since an earlier subassembly made from DOFL-fabricated NOR's had operated, it was concluded that the Sprague use of air-dry silver paint for electrical and mechanical connections, instead of the DOFL-employed conductive adhesive (ref 5), was at fault.

Several unpotted assemblies including a majority-vote circuit, a half-adder, and full-adder, and an oscillator were built from the NOR wafers. Some have now been operating for over a year. Two plug-boards containing 15 NOR's each were assembled to allow the rapid connection of specific logic networks (fig 2).

Several limitations in the 2D-NOR's as delivered were noted:

- (1) The units varied considerably in overall thickness.
- (2) The manufacturer used air-dry silver paint which may dissolve when the unit is subsequently encapsulated
- (3) A number of intermittent or failed stages attributed to bad connections were noted.
- (4) The leads of the units were tinned copper wire, and this frustrated experimentation on welded interconnection.

Weldability was not specified in the purchase order. The only specified characteristic was that the units operate properly when first received at DOFL.

In April 1959 negotiations were made to purchase 200 2D binary divider units (fig. 3). Sprague Electric Co. won the competitive bid, agreeing to deliver 200 2D binary divider units. A conductive adhesive similar to the one employed at DOFL would be used for all connections to the semiconductor devices. Nickel ribbon would be substituted for the tinned copper wire used in the NOR units. This use of nickel ribbon would both allow for welding, if desired, and contribute less height than round wire to the overall wafer dimensions.

It is the purpose of this report to (1) chronicle the delivery of the subject 200 2D binary divider units, (2) to describe the tests performed by DOFL on these stages, and (3) to discuss some of the subassemblies built from these stages and the interconnection schemes investigated.

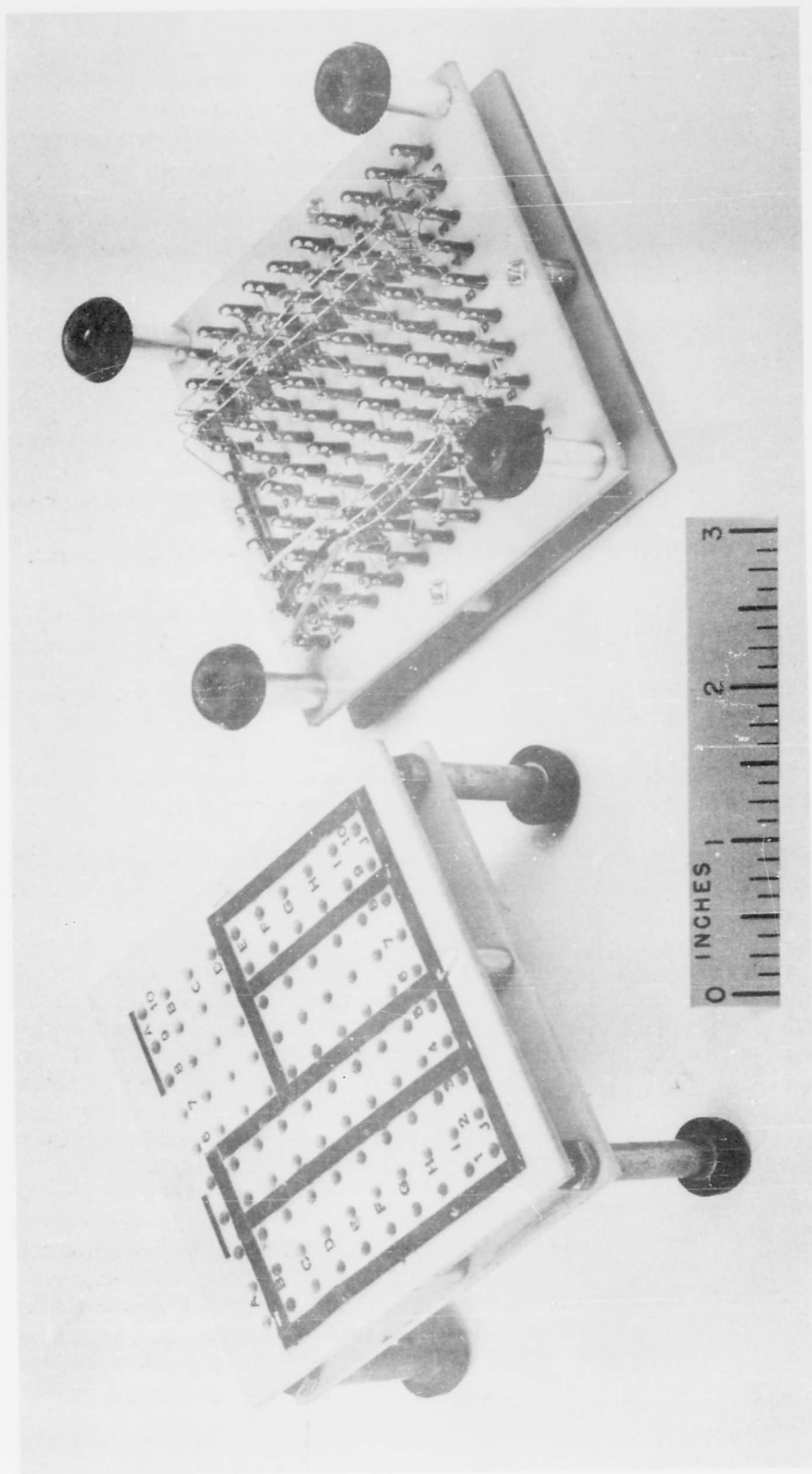


Figure 2. Top and bottom view of plug-boards each containing fifteen 2D-NOR circuit wafers.

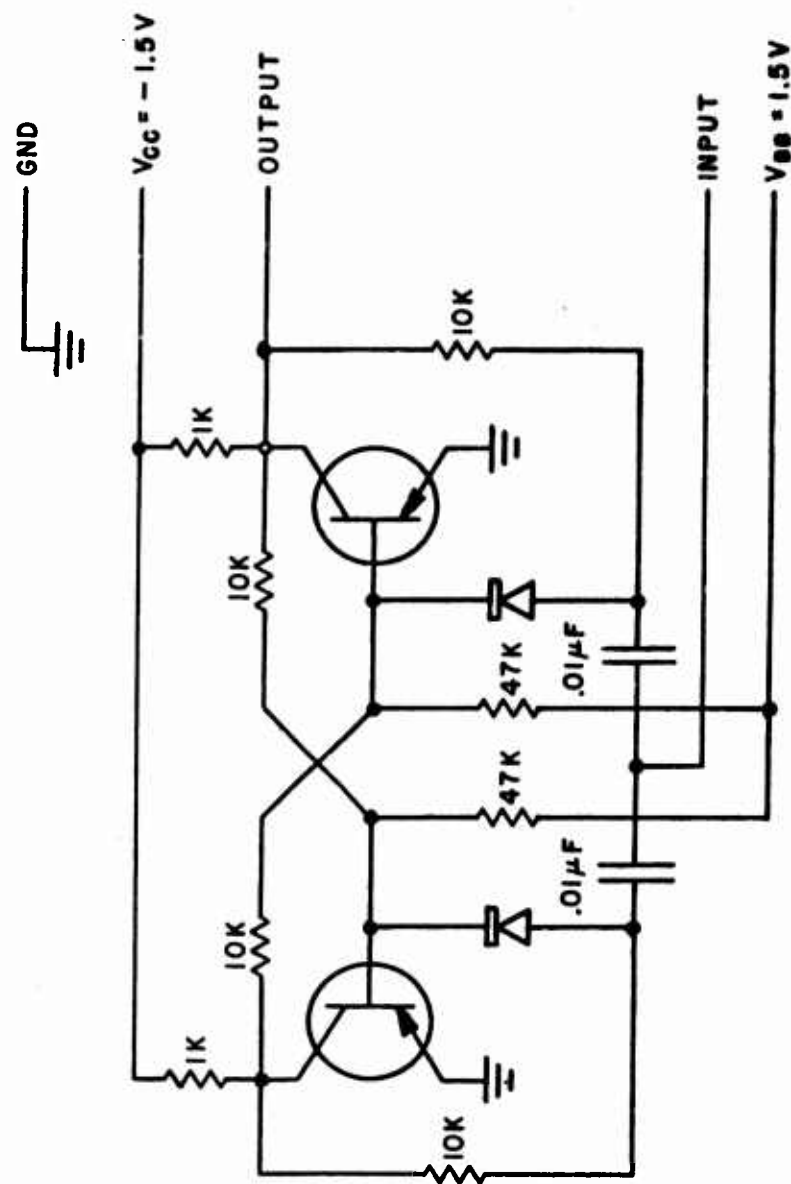


Figure 3. Schematic diagram of binary divider circuit.

## 2. EXPERIMENTAL METHODS

### 2.1 Shipment

The 2D-binary divider units were shipped from the Sprague Electric Co. to DOFL in lots varying in size from three to twenty-five units each. Each unit was separately packaged in tissue and then placed in a styrene box. A number of these boxes were then placed in a larger styrene box containing a desiccant. Figure 4 shows a typical box. The large box as delivered was taped closed with cellophane tape. One or more of the larger styrene boxes was packaged in a standard cardboard shipping carton. The delivery schedule is shown graphically in figure 5.

### 2.2 Unit Topology

The binary divider stages supplied by Sprague were fabricated on a high-K monolithic substrate (ref 6) from whence was derived the relatively high input capacitors required in the circuit. Other circuit elements were isolated from the high-K substrate by a screened low-K insulator (ref 7). The resistors were screened in place with a carbon-resin ink while the transistors and diodes were made from decased and inserted RCA 2N412 transistors. One half of a transistor sufficed where diodes were required.

The 200 delivered units were of three different topologies. The first three units had the layout shown in figure 6. The remaining 197 were about equally divided between the two layouts shown in figure 7. All units measured 0.500 x 0.500 in. in area and between 0.040 and 0.050 in. in overall thickness. They had nickel-ribbon leads and were each marked with an identification number.

### 2.3 Incoming Inspection

All units delivered to DOFL were measured to determine operating range in terms of loading and voltage endpoints. Figure 8 is a schematic of the apparatus employed. The starting parameters are given in the "Standard Condition" column of table I.

While all other parameters were maintained constant, each parameter in turn was varied until the unit under test failed to properly perform binary division. The total evaluation resulted in a minimum collector voltage ( $V_{cc \min}$ ), minimum load resistance ( $R_{L \min}$ ) maximum load capacitance ( $C_{L \max}$ ), maximum input resistance ( $R_{in \max}$ ), and maximum operating frequency ( $f_{\max}$ ) for each unit. A minimum bias voltage ( $V_{bb \min}$ ) or the fact that the stage would operate without bias was also established. Typical endpoint values are also shown in table I.

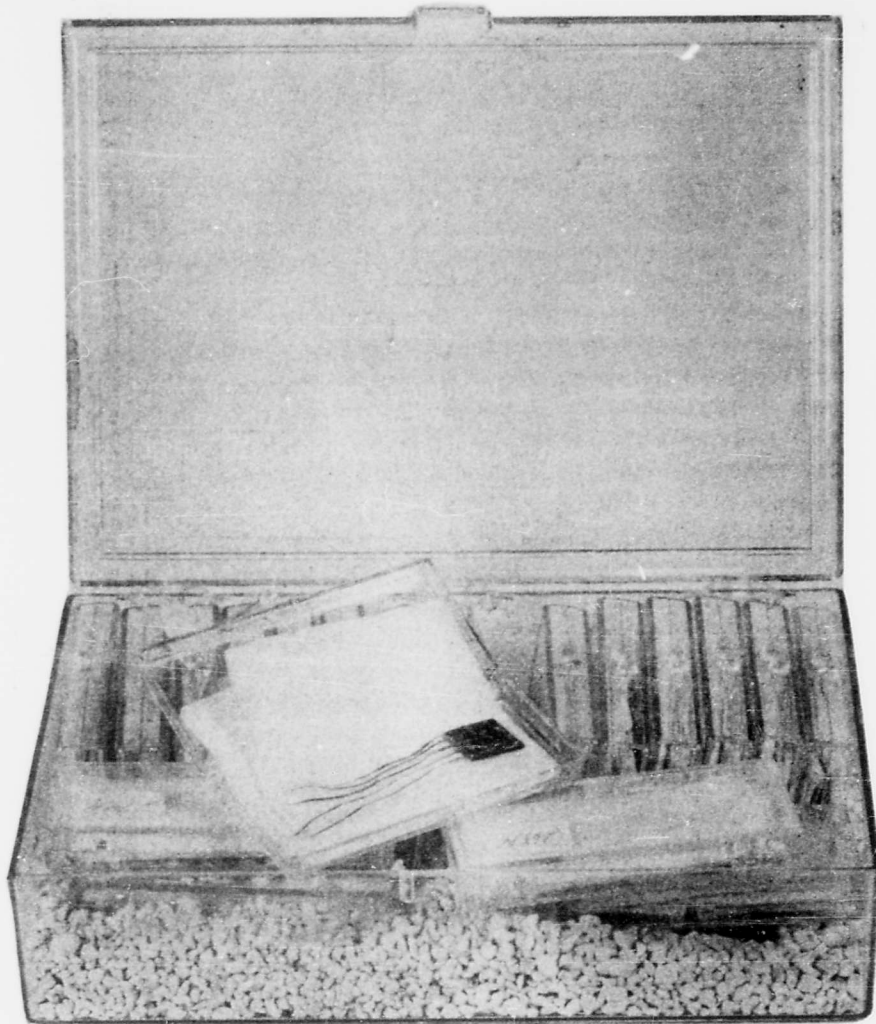


Figure 4. Method of shipment employed by Sprague Electric Company consisted of separate boxing of units and subsequent packing with desiccant in a larger box.

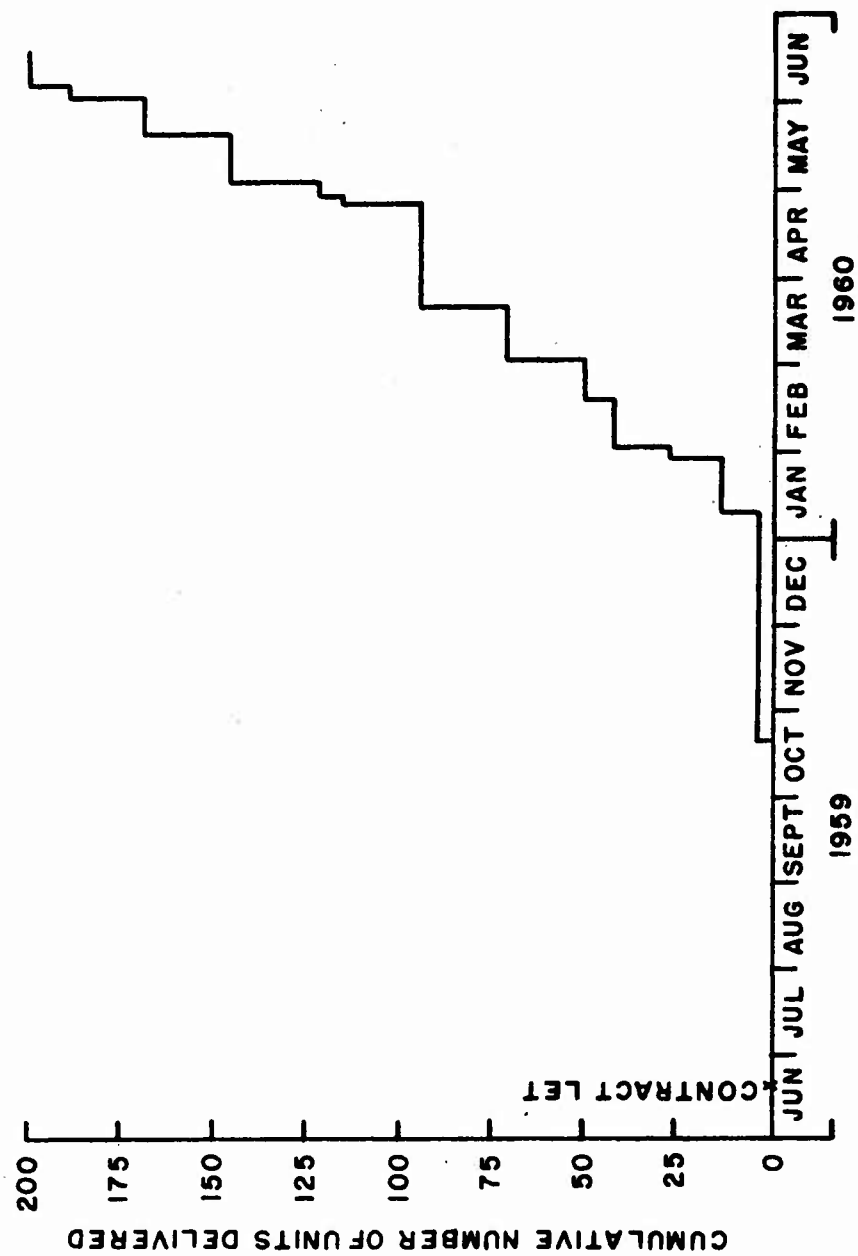


Figure 5. Delivery schedule on 2D-binary divider units from Sprague Electric Co.

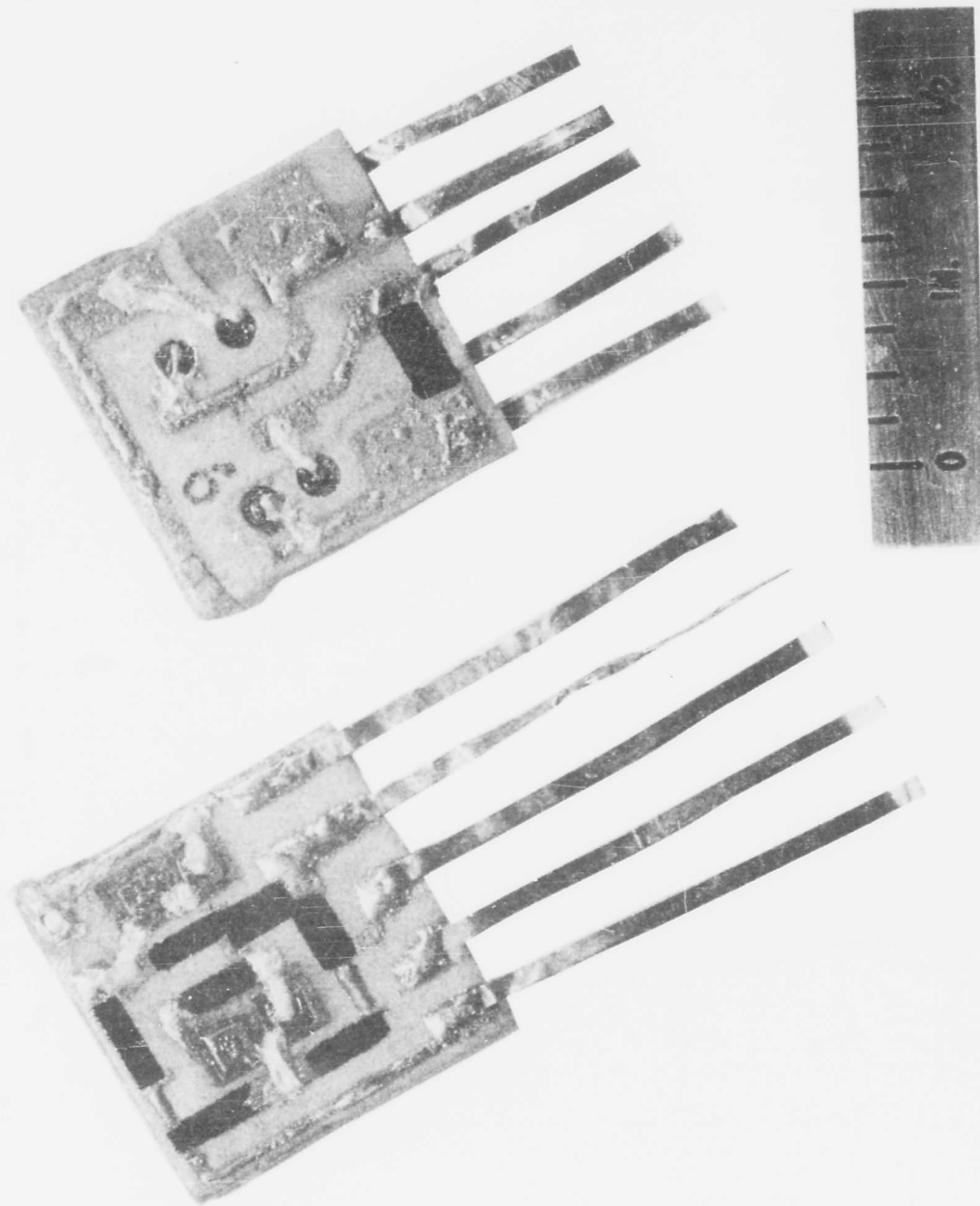


Figure 6. Layout of first three 2D-binary units delivered was of the type pictured above.

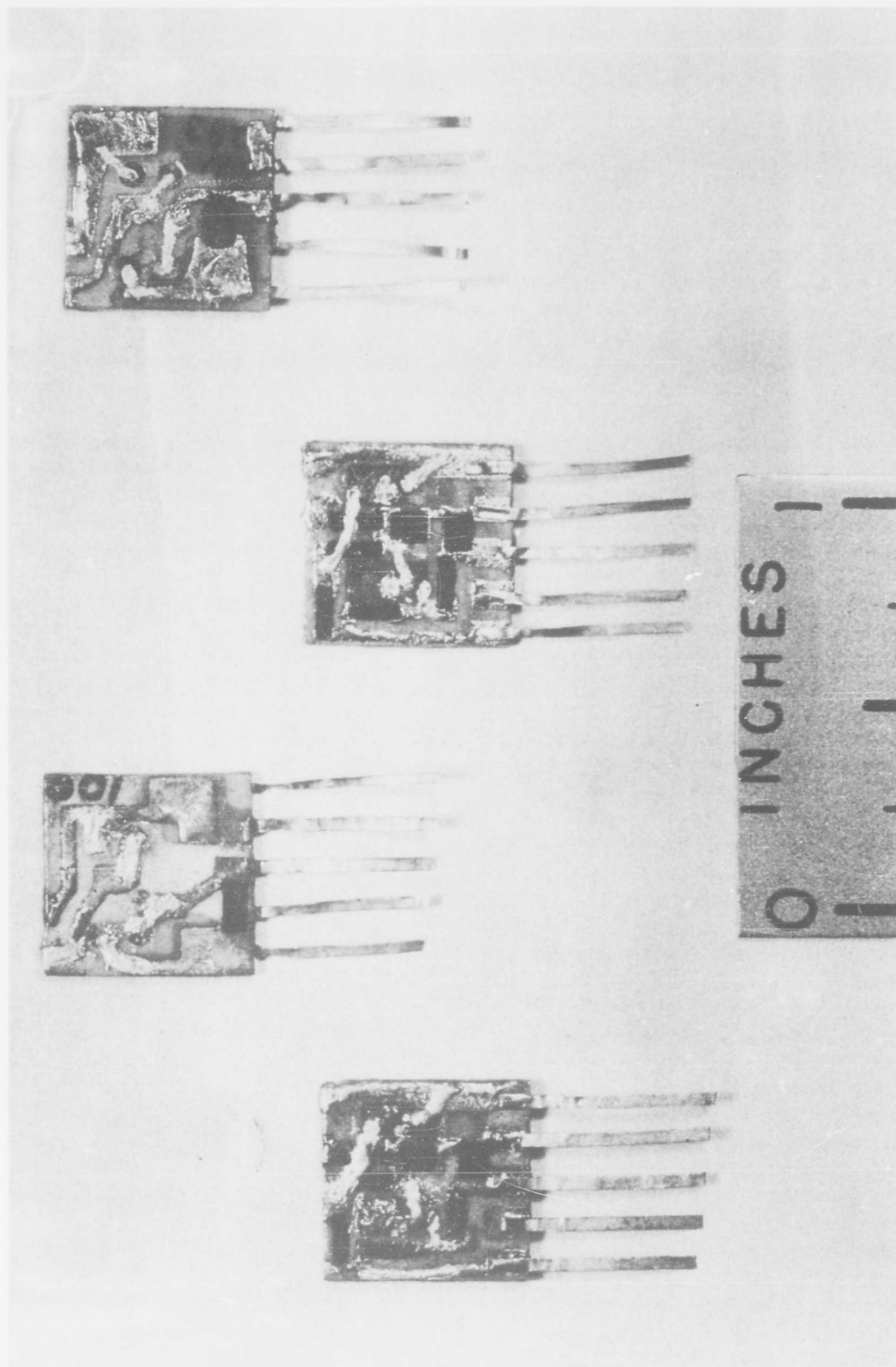


Figure 7. Remaining 197 2D-binary units were about equally divided between the two layouts pictured left and right above.

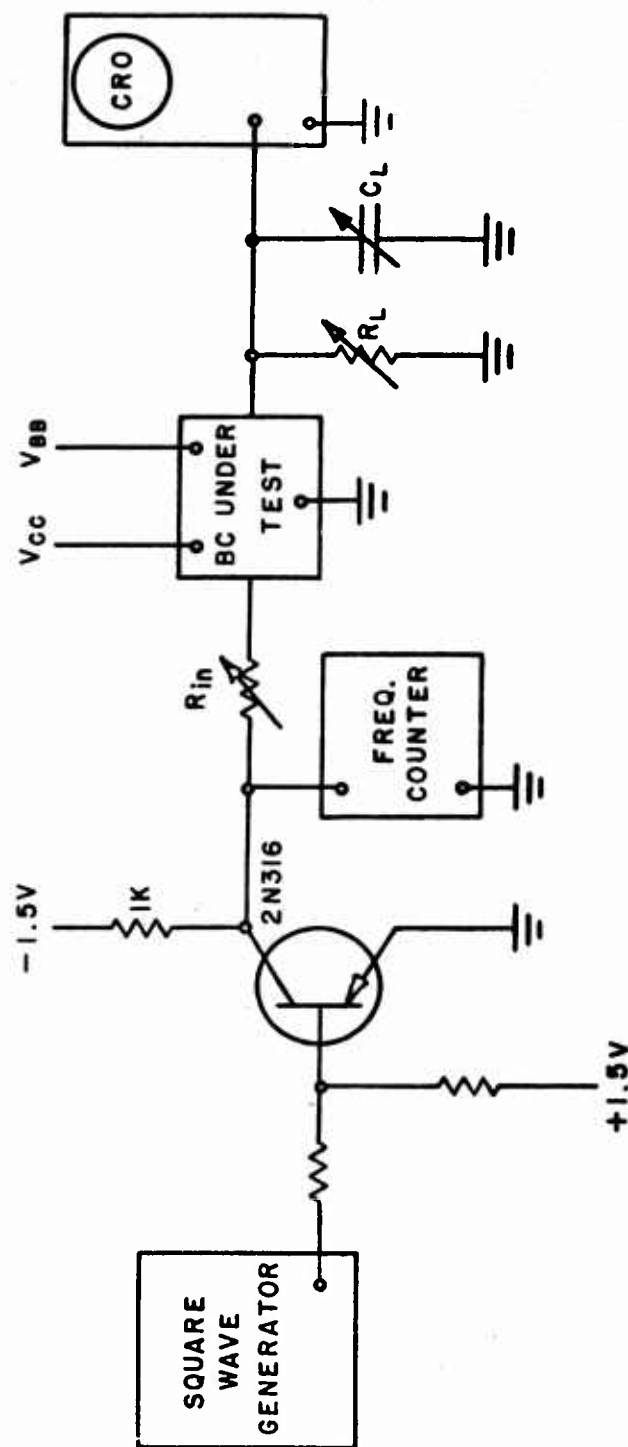


Figure 8. Block diagram of apparatus used for determining circuit margins on 2D-binary divider units delivered by Sprague Electric Co.

TABLE I. Test Parameters for 2D-Bi. . . Divider Gates

Parameter	Standard Condition	Direction Changed	Typical End Point
Collector supply voltage ( $V_{cc}$ )	1.5 volts (neg.)	Reduced	0.7 volt
Bias supply voltage ( $V_{bb}$ )	1.5 volts (pos.)	Reduced	(a)
Input drawing frequency ( $f$ )	1000 cps	Increased	25 kc
Load Resistance ( $R_L$ )	> 100 $k\Omega$	Reduced	800 $k\Omega$
Load Capacitance ( $C_L$ )	0	Increased	0.08 $\mu f$
Input Resistance in series with generator ( $R_{in}$ )	0	Increased	9 $k\Omega$
Input voltage ( $V_{in}$ )	1.5 volts peak to peak <sup>(b)</sup>	Not changed	---

(a) Most units operated properly at room temperature with no bias supply voltage.

(b) The most positive part of the waveform was held at ground potential.

Late in the delivery schedule another statistic was added to those already mentioned. This statistic was termed "spike height" and was a quantitative measure of the voltage swing associated with an unexpected and unwanted, but nevertheless present, voltage spike in the collector waveform of some of the units. Figure 9 shows the shape and phase location of the spike which is usually not apparent unless the bias voltage is reduced significantly below the nominal value.

Several binary divider units were placed in a temperature chamber and voltage and loading end-points were determined at various temperatures. Curves of these endpoints versus temperature for a typical unit are given in figure 10. Curves of  $\beta$  and  $I_{co}$  for the 2N412 transistor and a curve of the percentage change in capacitance of the substrate material employed by Sprague are given in figures 11 and 12, respectively. These will be useful in interpreting the shape of the curves given in figure 10.

## 2.4 Subassembly Construction

### 2.4.1 Deposited Metal Interconnection

The feasibility of encapsulating a stack of 2D wafers, facing off the protruding lead wires flush with the surface of the encapsulant, and subsequently interconnecting the desired wire cross-sections by metal deposition and selective etching had been demonstrated earlier (ref 4). With the 2D binary dividers received from Sprague it was necessary to determine if (a) they would survive epoxy encapsulation and (b) they could be successfully interconnected in the above manner.

Two 2D-binary divider plates were encapsulated in the manner shown in figure 13. The five lead wires on each stage were bent to form a U, with the ends of the wires allowed to protrude from the mold. After curing of the resin, the encapsulated units were tested to assure survival. Both units performed proper binary division and showed no significant variation in electrical margins. Next the U's were severed and connections were made with chemically deposited copper. One stage was working when they were tested again. The other stage was subjected to failure analysis and found to have a defective edge-silver connection on the wafer itself.

A nine-stage counter package was next attempted. The first unit was constructed using one live stage and eight dummies. Subsequently two all-live nine-stage counters were fabricated. The potting fixture and output connector employed are shown in figure 14 along with a completed unit. Side rails machined from cured epoxy resin were placed in a Teflon mold. A thin piece of cured epoxy was placed on the bottom of the mold to prevent the individual wafers from touching the

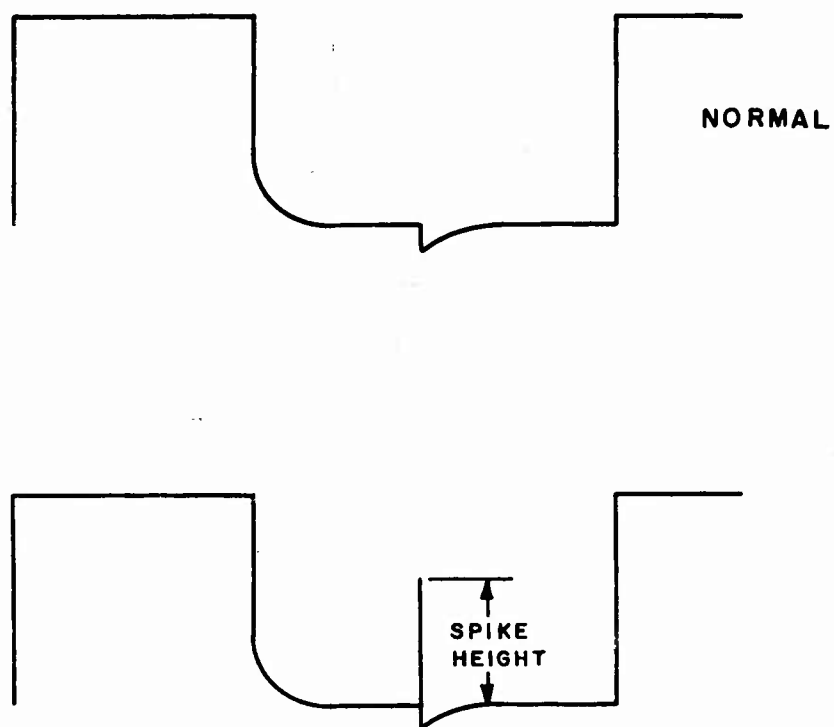


Figure 9. Binary divider output wafers: normal (top) and abnormal because of presence of undesired spike (bottom).

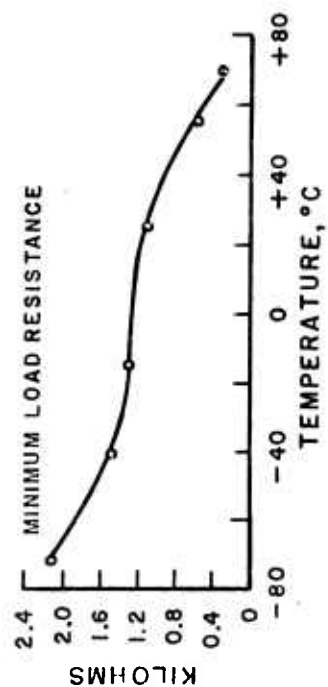
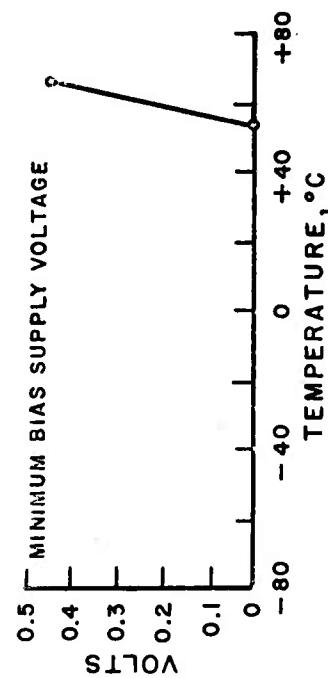
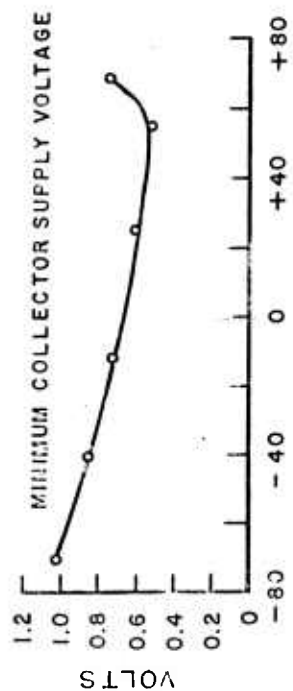
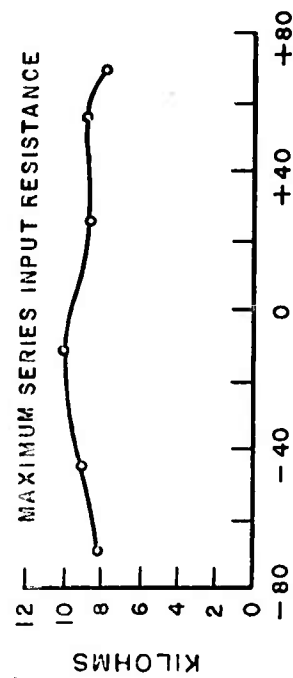
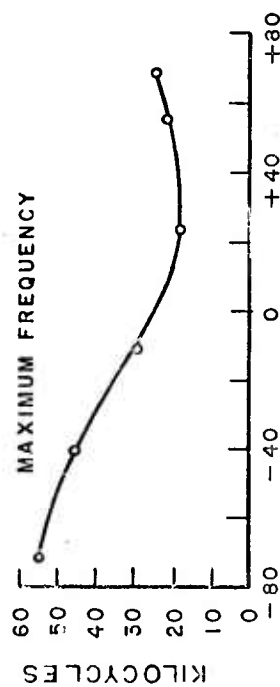
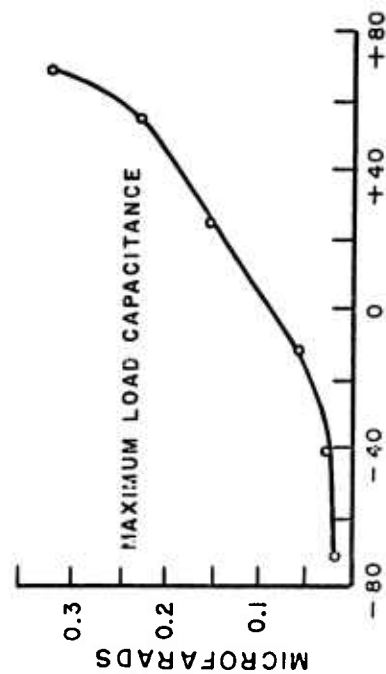


Figure 10. Frequency, voltage, and loading endpoints as a function of temperature for a typical 2D-binary unit.

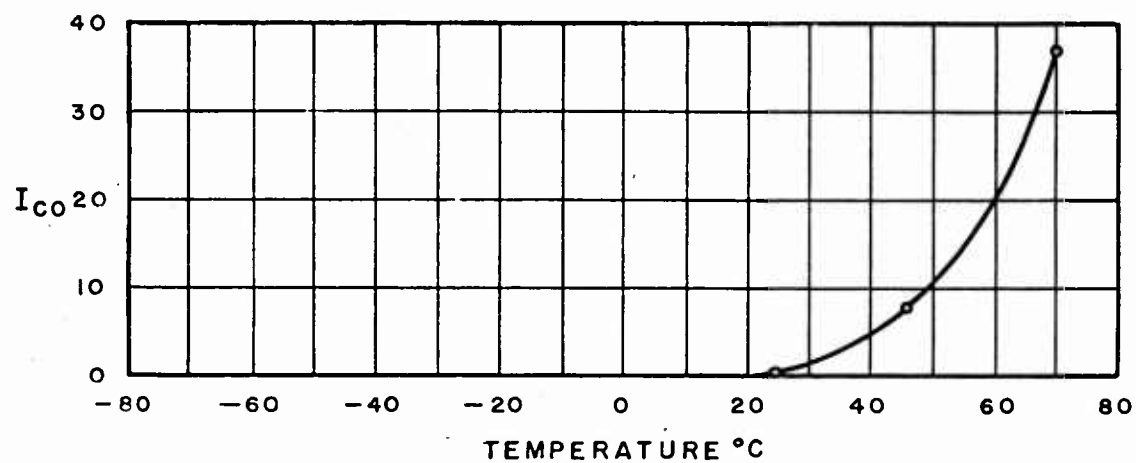
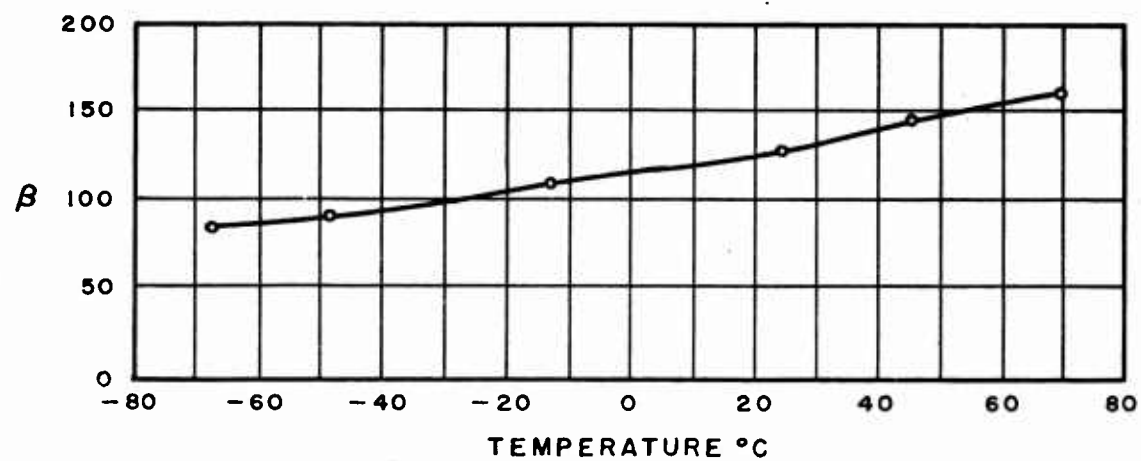


Figure 11. Current-gain ( $\beta$ ) and leakage current ( $I_{CO}$ ) as a function of temperature for a typical 2N412 transistor.

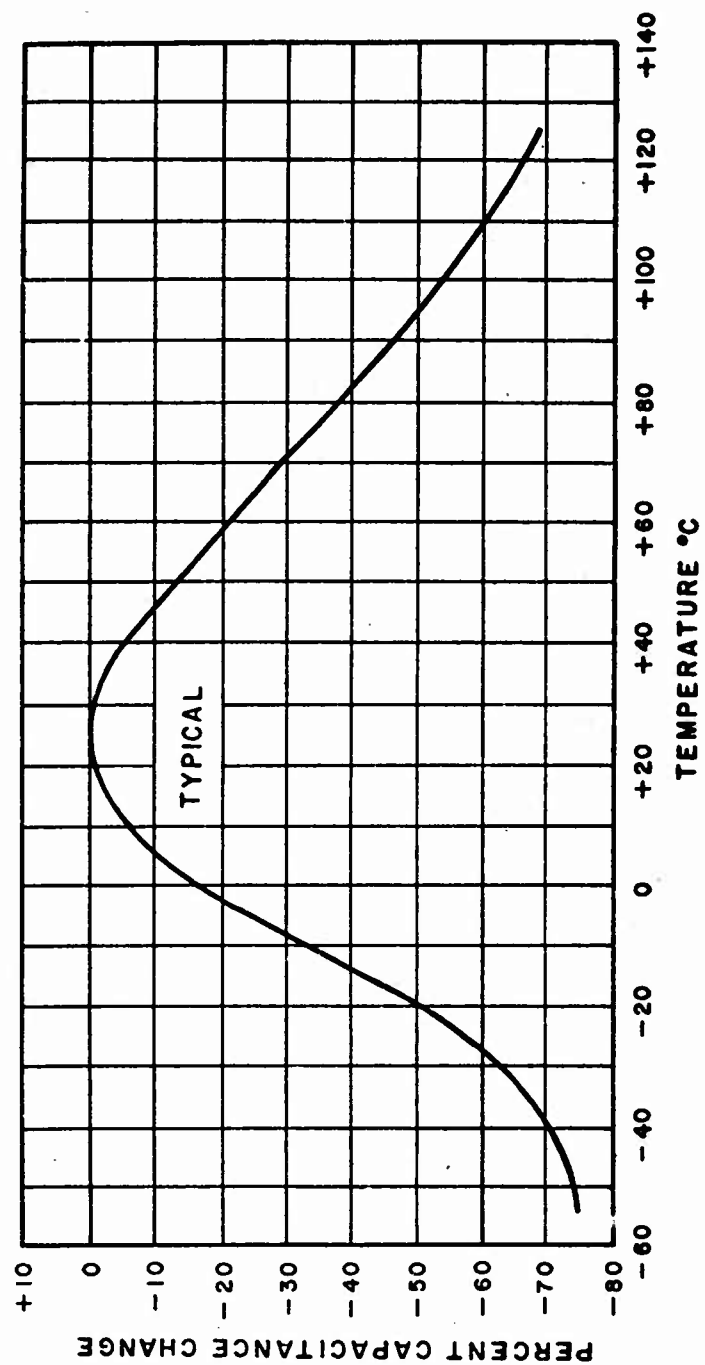
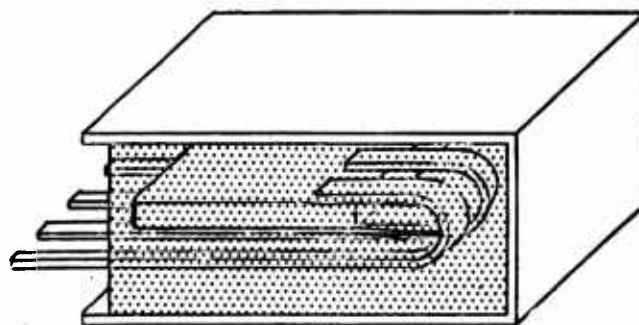
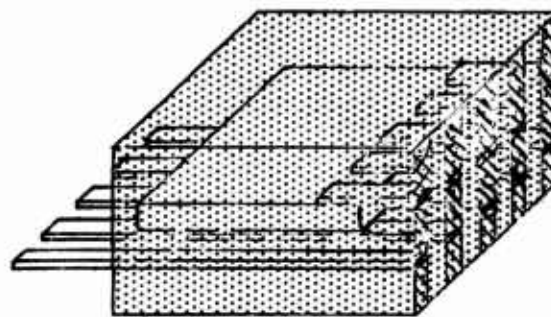


Figure 12. Capacitance change as a function of temperature for ceramic body used by Sprague Electric Co. as substrate of 2D-binary divider units.



ENCAPSULATED IN MOLD



REMOVED FROM MOLD, FACED  
OFF AND RECONNECTED WITH  
DEPOSITED COPPER

Figure 13. Initial test specimen employed to evaluate whether 2D-binary dividers would survive encapsulation and deposited metal interconnection.

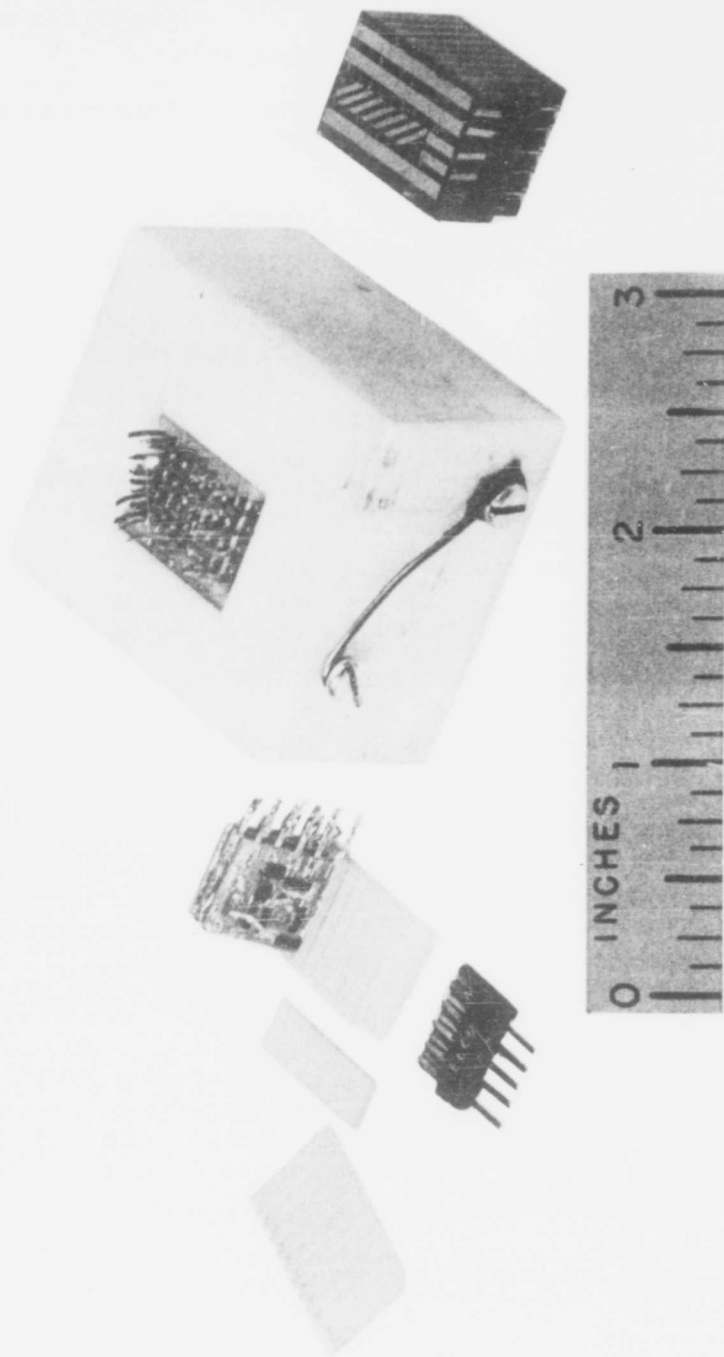


Figure 14. Potting fixture (center) employed in the fabrication of 9-stage countdown units (right).

bottom of the mold. A five-pin Elco-type 8101-5 connector and nine 2D wafers were inserted into the side rails with their lead wires protruding from the top of the mold. Epoxy resin was added and the units were allowed to gel overnight at room temperature and then cured for 2 hours at 80°C. All nineteen 2D-binary divider wafers survived potting as determined by electrical tests made via the protruding lead wires. After machining and applying deposited metal interconnections it was discovered that only about half the units were still operating.

Further measurements made on these encapsulated stages are reported under section 6, "Failure Analysis."

#### 2.4.2 Welded Interconnection

Several counters were assembled using welding techniques. The first structure employed is shown in figure 15. It consisted of a lucite chassis which allowed welded connections to be made 1/2 in. from the wafer bodies. If a wafer had to be replaced, it still had sufficiently long leads after cutting to enable failure analysis.

This structure was later modified to give a more realistic picture of the total size of a 2D assembly. The later structure shown in figure 16 is an 11-stage counter capable of being hermetically sealed. Figure 17 shows a weld-and-roll method of making connections that was employed in the fabrication of the latter unit.

#### 2.5 Environmental Testing

##### 2.5.1 Storage at 65-80°C in Vacuum

Two 2D-binary divider units were mounted on a header and sealed in a glass container that was subsequently evacuated (fig. 18). The loading, voltage, and frequency endpoints were measured as noted previously and the entire assembly was placed in an oven maintained between 65 and 80°C. Periodically the glass-encased units were removed from the oven, allowed to cool to room temperature, and remeasured. Results obtained to date are tabulated in table II.

##### 2.5.2 Operation in Vacuum at Room Temperature

A second glass envelope was constructed containing a countdown assembly composed of ten 2D-binary dividers interconnected by welding (figure 19). This assembly, initially constructed on 2 March 1960, was vacuum sealed and permanently connected to a power supply on 28 June 1960, and allowed to operate continuously at room temperature.

Improper counting was noted from 30 June 1960 on. Instead of the proper countdown of 1024:1, the improper count of 512:1 occurred. The failure was attributed to one defective stage in the assembly which

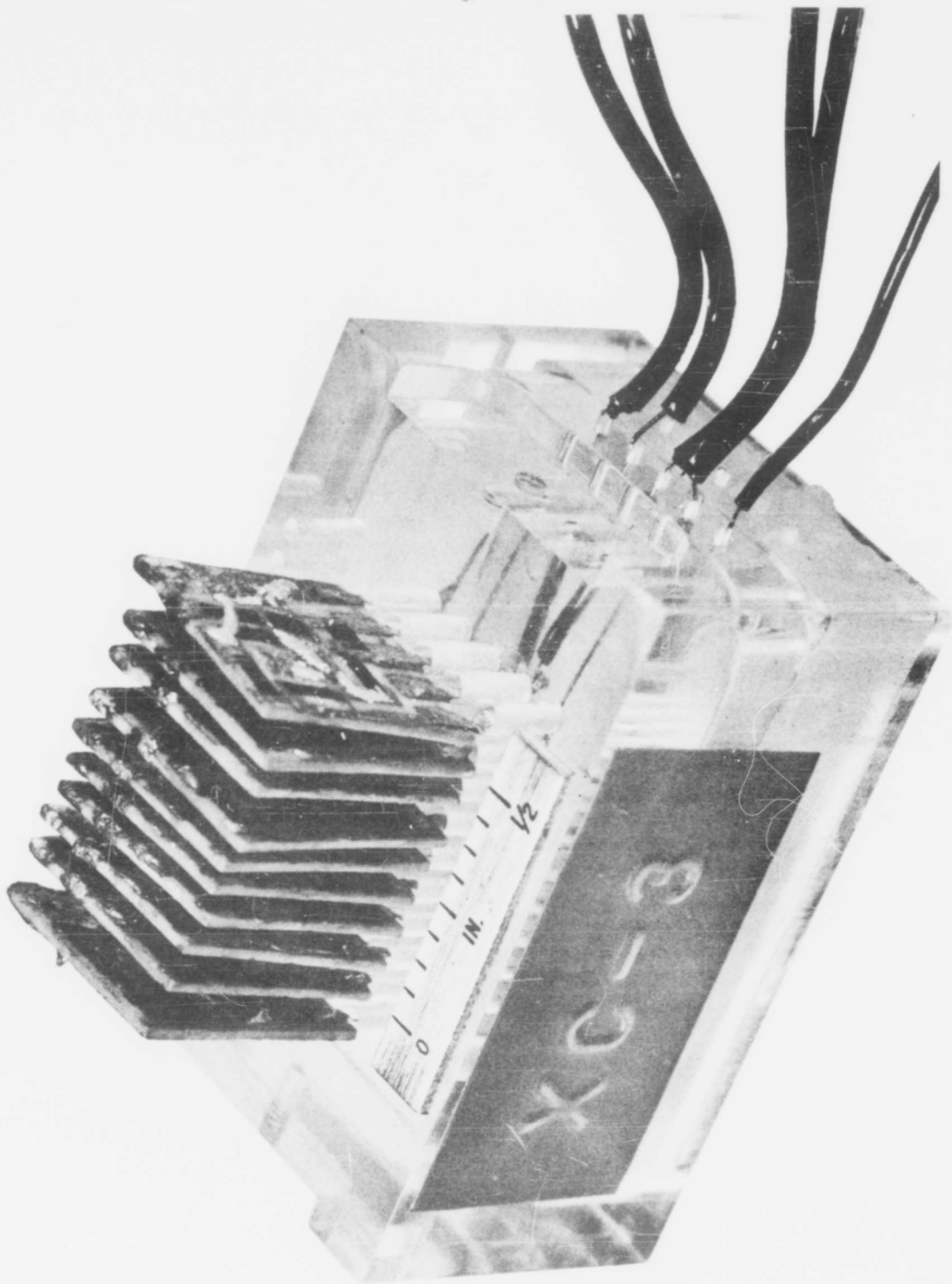


Figure 15. First structure employed in assembling binary counters using welding techniques allowed 1/2-inch of lead length to remain on each wafer.

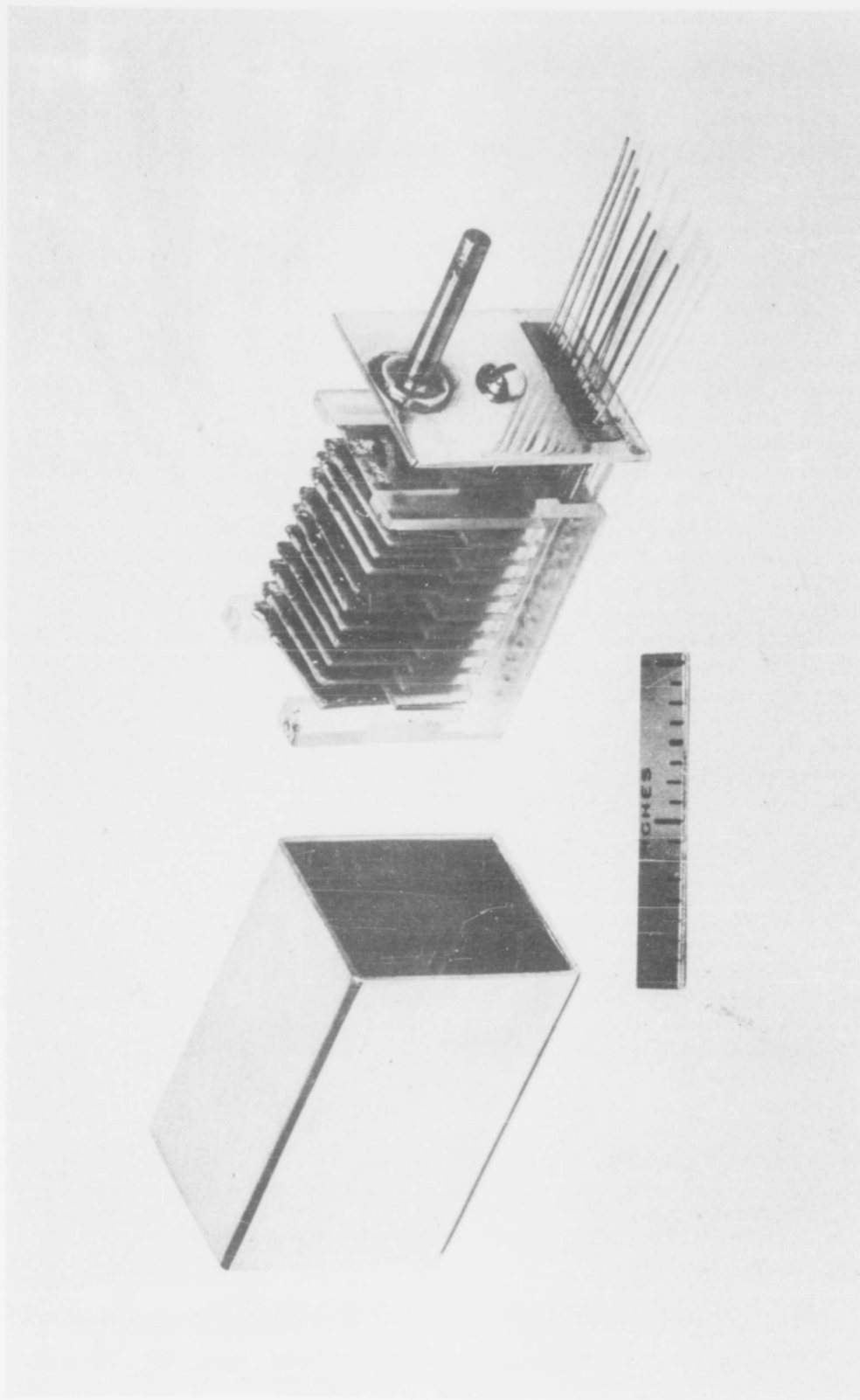


Figure 16. An 11-stage countdown unit assembled by welding techniques and capable of being hermetically sealed.

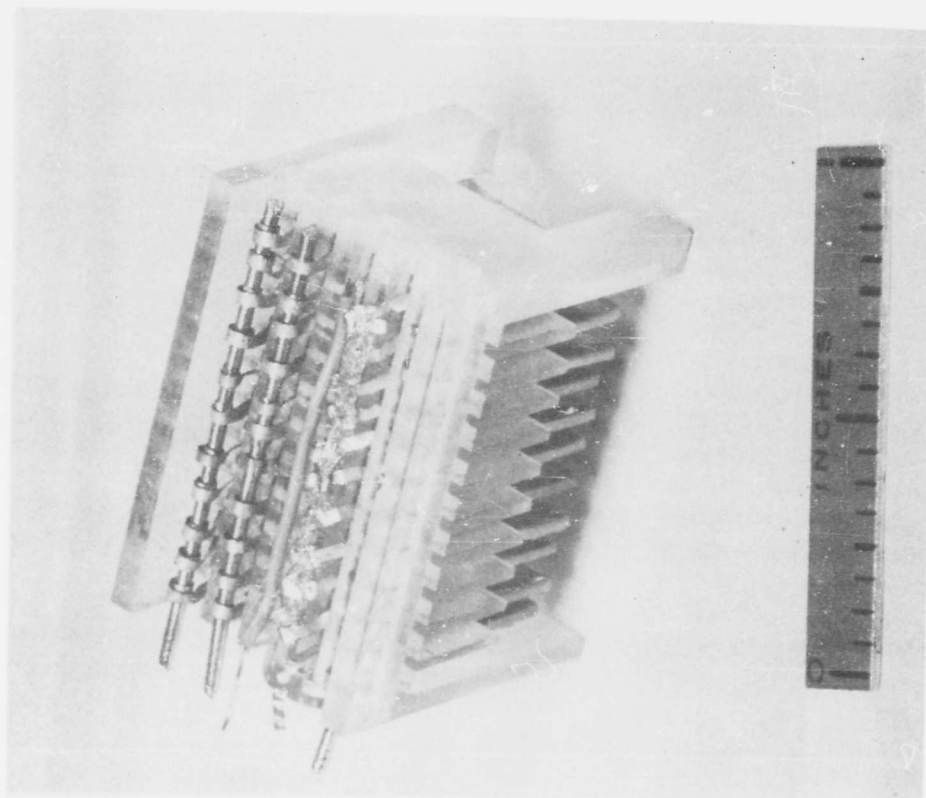
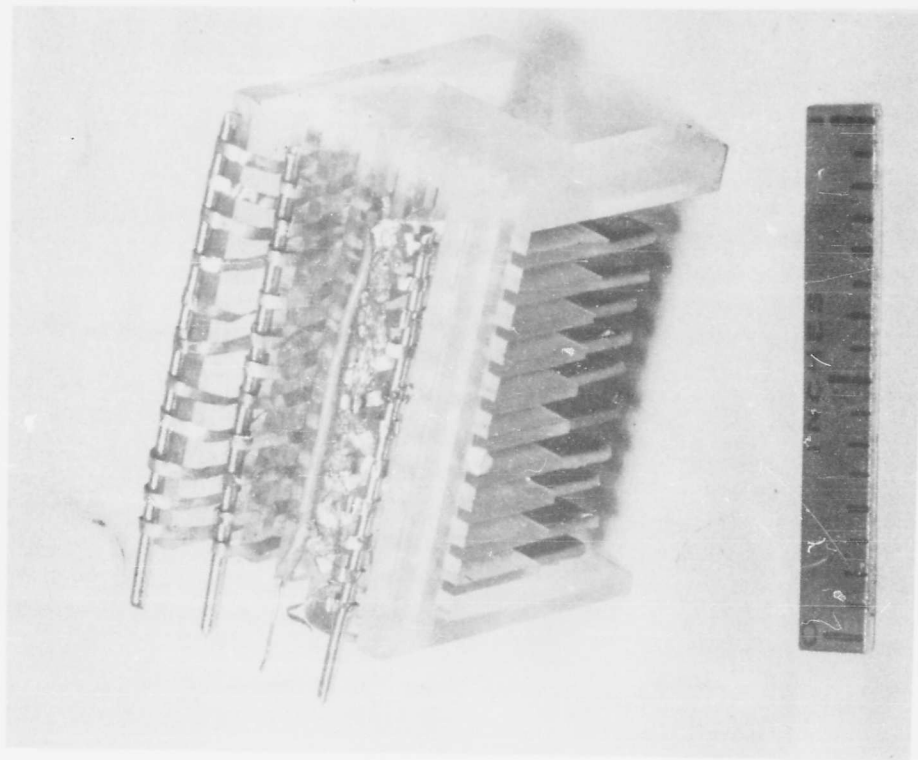


Figure 17. 2D-wafers with nickel ribbon leads are spotwelded to various interconnection rods (left) and the rods are rolled down flush with the back of the plastic block (right).

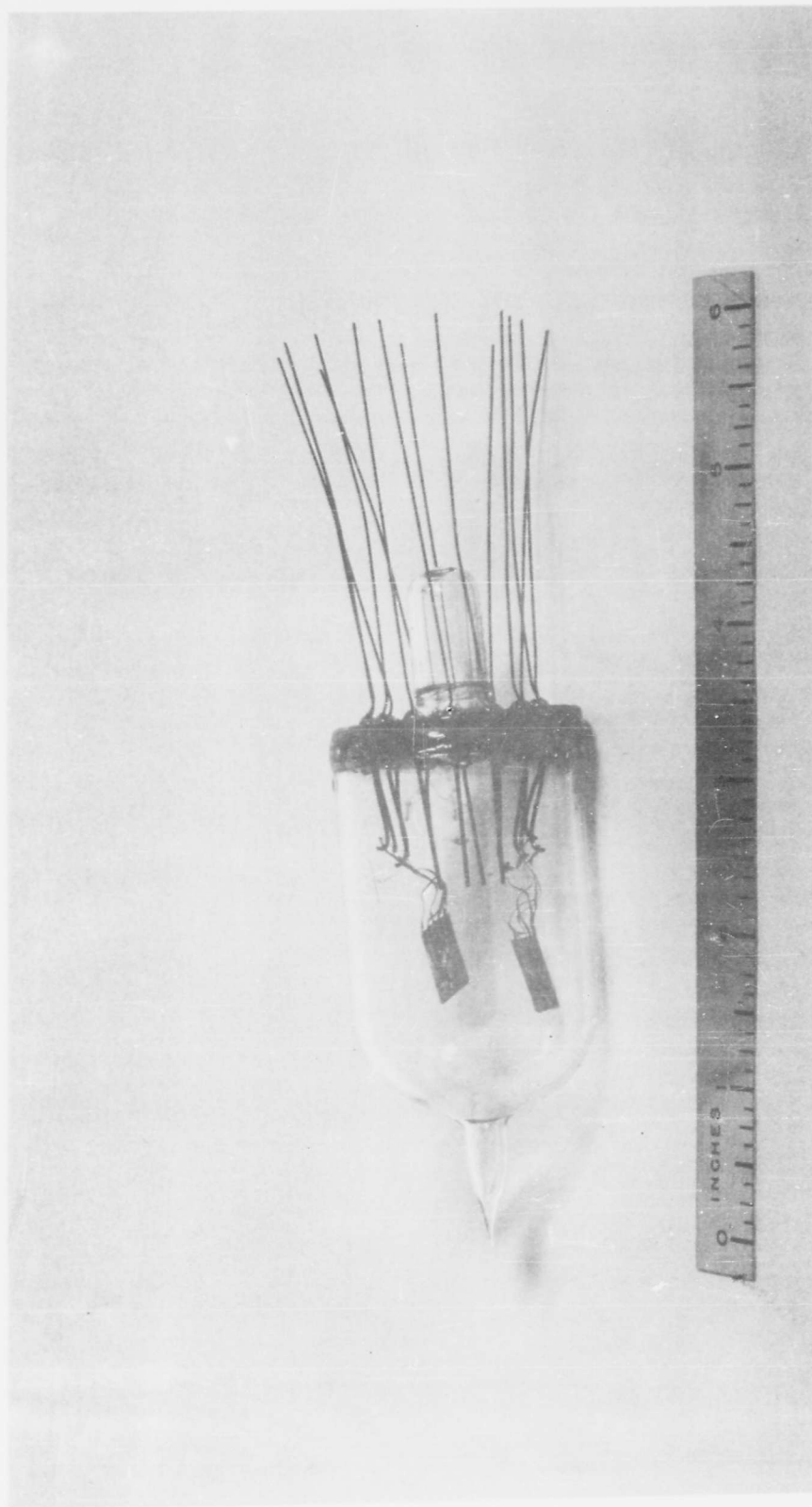


Figure 18. Hermetically sealed glass envelope employed in testing long-time high temperature vacuum storage of two 2D-binary divider units.

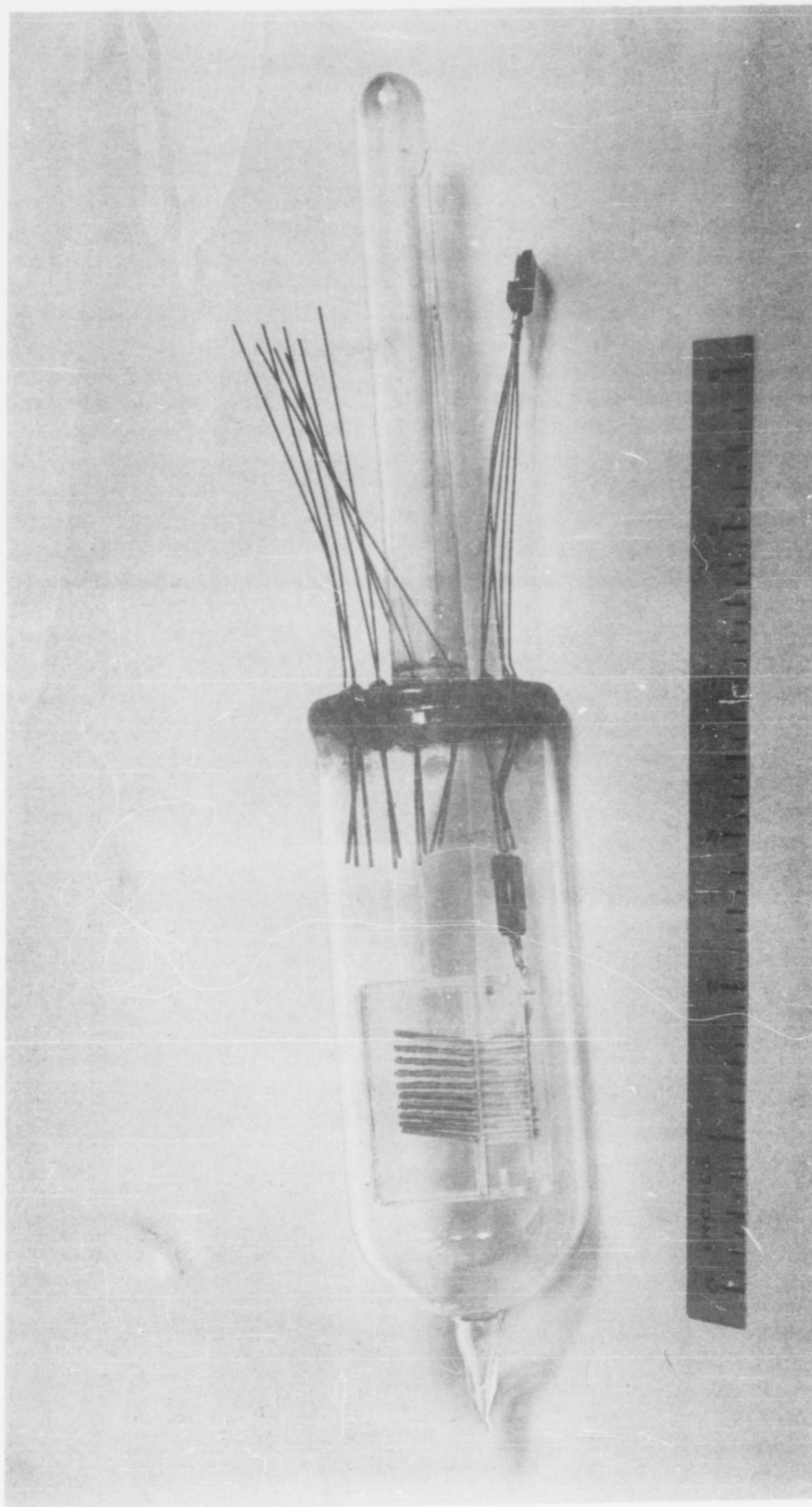


Figure 19. Hermetically sealed glass envelope employed in testing long-time room temperature operation of a 10-stage countdown assembly.

Table II. Circuit margins of two 2D-binary divider units stored at 65 - 80°C and measured at room temperature.

Unit No. 86

Date	Temp., °C	Min. $V_{cc}$ volt	Min. $V_{bb'}$ volt	Max. f kc/sec	Max. $R_{in}$ k ohms	Min. $R_L$ ohms	Max $C_L$ $\mu f$	Spike ht. at $V_{bb}=0$ , volt
2/29/60 <sup>(a)</sup>	25	0.71	(c)	23	8.2	960	0.1	---
3/2/60 <sup>(b)</sup>	27	0.71	(c)	24	8.3	840	0.1	---
6/30/60	27	0.71	(c)	14	---	---	---	0.45
7/27/60	23	0.73	(c)	12	---	---	---	0.28
10/20/60	22	0.76	(c)	21	9.1	1000	0.12	0.30
12/5/60	24	0.76	(c)	18	9.0	1100	0.12	0.24
1/9/61 <sup>(e)</sup>	27	0.98	0.12	20	8.3	2100	0.084	---

Unit No. 109

2/29/60 <sup>(a)</sup>	25	0.81	(c)	26	9.0	1700	0.068	---
3/2/60 <sup>(b)</sup>	27	0.76	(c)	27	9.0	1300	0.068	---
6/30/60	27	0.77	(c)	16	---	---	---	0.20
7/27/60	23	0.79	(c)	14	---	---	---	0.15
10/20/60	22	0.84	0.14	22	11.4	2000	0.08	(d)
12/5/60	25	0.89	(c)	19	10.0	2600	0.071	0.24
1/9/61 <sup>(e)</sup>	27	1.05	(c)	20	9.6	4000	0.058	0.30

(a) Before hermetically sealing

(b) After hermetically sealing; Units put in oven on this date

(c) Unit operates properly without  $V_{bb'}$

(d) Unit did not operate properly at  $V_{bb} = 0$ .

(e) The oven was disconnected for an indeterminable amount of time between 12/5/60 and 1/6/61.  
 --- Not measured.

was dividing by one instead of two. Since it was not convenient to unseal the package at the time, the assembly was allowed to continue in operation.

On 25 November 1960, after 3600 hr of continuous operation, the glass envelope was opened and the countdown assembly examined. Stage 7 of the assembly was found to be mechanically defective; it divided by one instead of two.

### 2.5.3 Operation in Air at Room Temperature

Twenty-five 2D-binary divider units were soldered to an etched wiring board laid out to form five 5-stage countdown assemblies operating in parallel. The physical appearance of this life test arrangement (fig. 20) led to the name "Bingo Board." Voltage was permanently attached to the 25 units under test and each of the countdown assemblies was driven by the same input signal which during the testing period was varied from 60 cps to 12,000 cps, to 10,000 cps. These test frequencies were determined by what other circuitry was currently under test.

As binary dividers failed, they were removed from the Bingo Board and subjected to failure analysis. New units were soldered into the Bingo Board to replace those that failed. To date, five units have failed in a total of 3000 hr (75,000 unit hours). One failed after 400 hr, two after 500 hr, one after 1300 hr, and one after 1800 hr continuous operation.

The parallel operation of the five countdown assemblies was intended to see how long an in-phase operation could be maintained. Early in the program, transients in the power supply, or the pickup in the lead wires never allowed more than 30 hr to pass with all five units in phase. Recently the transistorized power supply was replaced by batteries and significantly longer times of continuous in-phase operation have been recorded. Shielding of the Bingo Board appears necessary to rule out external transients as a contributing factor to loss of phase.

### 2.6 Failure Analysis

It was noted over a period of time that some 2D-binary divider units would fail, i.e., they would no longer perform binary division. Whenever such an improperly operating unit was detected it was removed from the subassembly into which it had been built and subjected to failure analysis.

The analysis procedure was designed to ferret out the defective part on the circuit wafer and discover the failure mechanism that produced it. Although the analysis procedure was continually being modified as a result of applying and improving it, it consisted basically of three steps.

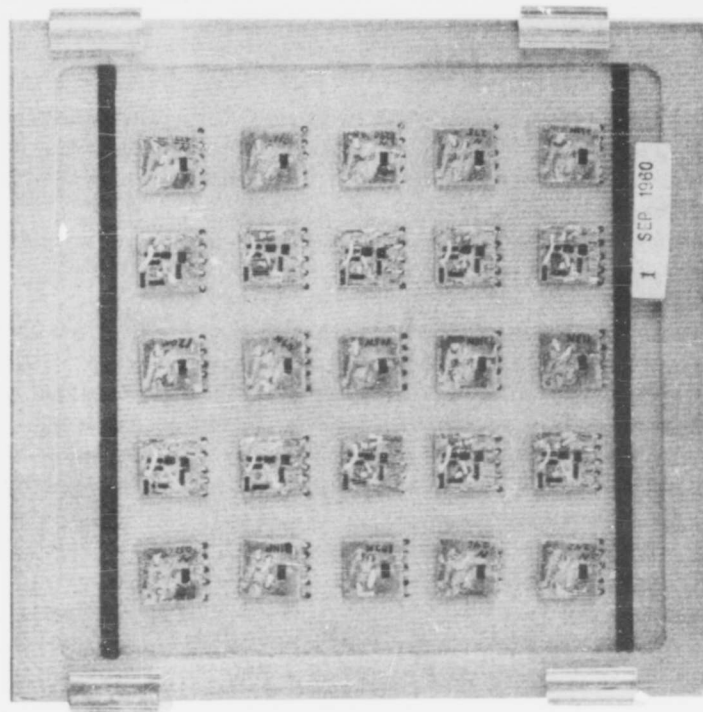
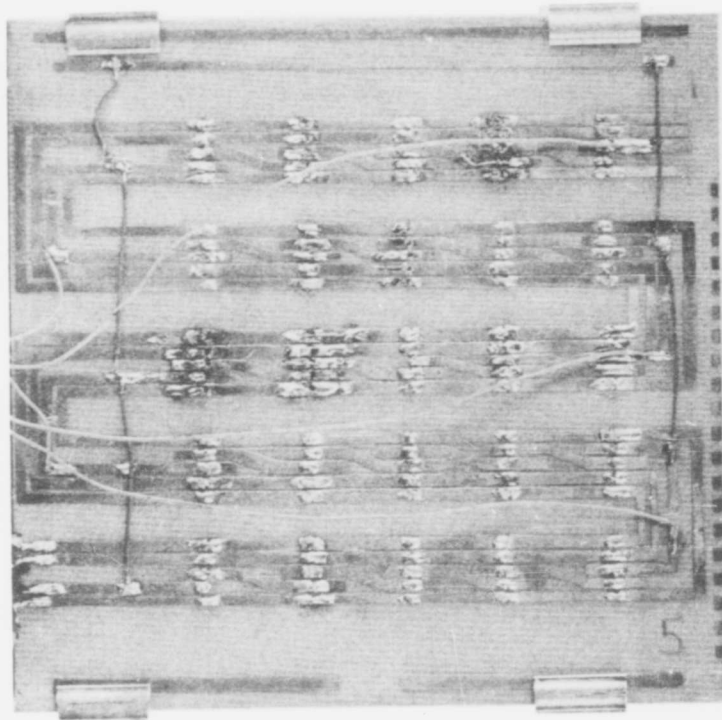


Figure 20. "Bingo Board" life test assembly holds 25 1/2-inch square 2D-binary dividers which are kept in continual operation at room temperature.

The first step was to examine the improper waveform on an oscilloscope. This would often reduce the number of possible failure mechanisms considerably. The second step was to make resistance measurements between the various leadout wires. In the case of the 2D-binary divider wafers there are five leadout wires: (1) ground, (2)  $V_{cc}$ , (3) output, (4) input, and (5)  $V_{bb}$ . The most important of these are the first three, since resistance measurements between the input lead and all others is very high unless a capacitor is shorted (this has not occurred as yet), and resistance measurements between  $V_{bb}$  and all others must as a consequence of the circuit include the bias resistors of 47 kohm each.

Experience has shown, however, that steps one and two alone, in most cases, cannot completely isolate a circuit fault and some form of internal probing becomes necessary. Step three consists of measuring resistances between the electrodes attached to the semiconductor devices in the circuit wafer. The probing is done by attaching ordinary sewing needles to the leads of an ohmmeter by means of miniature alligator clip leads. Since many of the resistances in the binary divider are nonlinear with voltage, the exact values of resistance measured will be a function of the ohmmeter and ohmmeter scale employed for the measurement. A triplet Model 310 meter on its X10 scale was used. When making measurements at the semiconductor electrodes, it is wise not to probe directly over the semiconductor devices because a little too much pressure on the needle might crack the crystal or rupture the semiconducting junction. It is always possible to make a safer measurement by backing away along a conducting path leading to the junction. The only exception to this is when it is suspected that the conducting path itself is defective.

A listing of the failure mechanisms associated with the 25 units which have so far proved defective is given in table III; complete diagnoses are not available on all units. One unit was shipped out of DOFL and another destroyed before analysis. Four other units are exhibiting an erratic failure mechanism and so far have not remained in the failed state long enough to permit analysis.

The binary divider units which failed in the encapsulated 9-stage countdown units interconnected by deposited metal could only be analyzed by steps one and two of the analysis procedure, since needle probing of individual wafers was impossible. For this reason analysis is incomplete and these failures have not been included in table III. It is suspected that most failures of encapsulated units resulted from mechanical damage probably introduced during the facing-off operation.

## 2.7 Equipment Construction

The only complex equipment attempted so far has been a modified Copperhead timer. The Copperhead timer is a digital electronic program timer which is intended to replace synchronous motor mechanical timers in many missile applications. It performs the same functions as a mechanical timer having many cam positions

Table III. Tabulated results of failure analyses performed on defective stages

Unit no.	Delivered to DOFL	Improper operation first noted	Diagnosis completed	Failure mechanism
123	1/29/60	2/28/60	2/28/60	Discontinuity in edge silver near output lead <sup>(f)</sup>
110	1/29/60	2/15/60	3/7/60	Open conductive adhesive connection
73	1/13/60	2/8/60	3/14/60	Bad contact at collector of non-output transistor, low diode backresistance and collector-emitter short.
126	2/2/60	3/2/60	3/14/60	Low diode backresistance
139	2/2/60	3/15/60	10/14/60	Poor contact between base tabs on diode and non-output transistor
50N	3/2/60	4/22/60	7/5/60 <sup>(b)</sup>	"Very low transistor reverse resistance (possible mechanical damage)"
144	3/2/60	4/20/60 <sup>(?)</sup>	7/5/60 <sup>(b)</sup>	"High resistance connections to semiconducting elements"
C	1/13/60	4/22/60	(c)	---
99	1/13/60	4/7/60	7/5/60 <sup>(b)</sup>	"High resistance connections to semiconducting elements"
7N	3/21/60	4/22/60	7/5/60 <sup>(b)</sup>	"Very low transistor reverse resistance (possible mechanical damage)"
6(Lot I)	10/20/59	4/22/60	7/5/60 <sup>(b)</sup>	"High resistance connections to semiconducting elements"
74	3/21/60	4/22/60	7/5/60 <sup>(b)</sup>	"Low diode and transistor reverse resistance"
104N	5/2/60	5/13/60 <sup>(a)</sup>	7/5/60 <sup>(b)</sup>	"Low transistor reverse resistance"
292N	6/1/60	7/5/60 <sup>(?)</sup>	7/5/60 <sup>(b)</sup>	"Low diode reverse resistance"
301N	6/1/60	7/5/60 <sup>(?)</sup>	(d)	Not evaluated: Used in inert stack of Ft. Knox exhibit
334N	6/1/60	7/15/60	7/15/60	Poor contact between base tabs on diode and non-output transistor

349N	6/6/60	9/12/60	10/14/60	Low diode back resistance
220N	5/2/60	9/12/60	11/17/60	Poor contact at collector of non-output transistor
371N	6/1/60	9/12/60	10/14/60	Open contact to emitter and emitter-collector short
149	4/27/60	9/12/60	10/13/60	Very low transistor reverse resistance; possibly also in diodes
310N	5/19/60	9/19/60	(e)	
254N	6/2/60	9/22/60	(?) (c)	
366N	5/19/60	10/7/60	(c)	
195N	5/2/60	10/7/60	11/17/60	Poor contact at collector of non-output transistor
308N	6/1/60	11/10/60	(c)	

(?) Date is an estimate

- (a) failed during initial acceptance testing
- (b) given to Sprague on date indicated; diagnosis of failure mechanism given in quotes is that reported by Sprague
- (c) diagnosis still pending; failure is of an intermittent nature
- (d) not evaluated; used in inert display
- (e) not evaluated; cracked during removal from assembly
- (f) an encapsulated stage.

and has the additional advantages of much higher accuracy and an ability to be preset remotely immediately before launching the missile. Several reports on this timer built by "hearing aid" miniaturization techniques have been issued (refs 8, 9).

Since a large portion of the timer is composed of binary divider stages, it was a natural item to attempt fabricating by 2D techniques. A block diagram of the timer is shown in figure 21.

It was possible to immediately begin construction of the 11-stage countdown and 11-stage counter blocks. The absence of reset diodes on the 2D-binary divider units, presently being fabricated, necessitated adding these externally. The Y-input was eliminated initially and then built using tiny commercially available parts. The oscillator was also constructed using commercially available parts. Diode logic was employed in place of the NOR logic employed in the original timer for the count sensing gates.

The assembly was breadboarded and it is shown in figure 22. A block diagram of this modified timer is shown in figure 23.

### 3. DISCUSSION

A contract for the fabrication and delivery of 200 2D-binary dividers was let to the Sprague Electric Co. on 25 June 1959. As can be seen in figure 5, the first units were delivered on 20 October 1959 and the entire order was completed by 10 June 1960; this demonstrates the ability of qualified industry to set up a 2D line and begin delivery of units within several months.

The use of a monolithic high-k body as a substrate for 2D-binary dividers was demonstrated. The complete absence of capacitor failures testified to the suitability of the Sprague technique. The only drawback to this technique is that the substrate thickness and hence the total unit thickness is slightly increased over the DOFL method of steatite substrates and inserted capacitor wafers.

The schematic pictured in figure 8, for incoming inspection testing, evolved gradually during the testing period. The inverter circuit placed between the square wave generator and the binary divider under test was found to be necessary because of the extreme sensitivity of several of the measured parameters, particularly  $f_{max}$  and  $R_{in max}$ , to the level of the input signal. It was difficult to hold the voltage of the input signal constant by adjustment of the attenuator on the generator even when using a voltmeter. The inverter circuit, the collector voltage of which could be set quite accurately, gave constant amplitude, output even with large variations in output level from the square wave generator.

The "spike" in figure 9 was an unwelcome but explainable phenomenon. Any of the following conditions could contribute to a spike

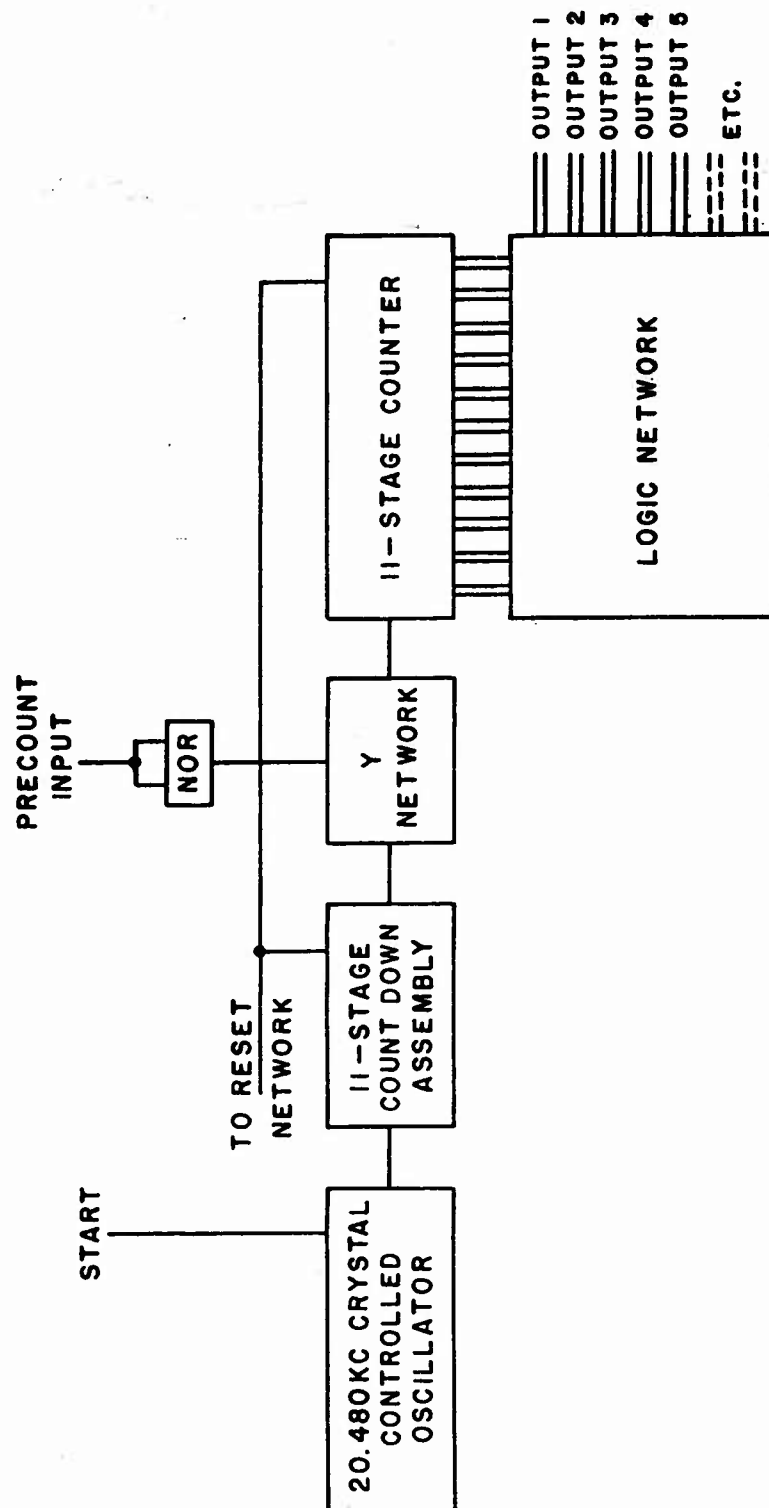


Figure 21. Block diagram of Copperhead timer.

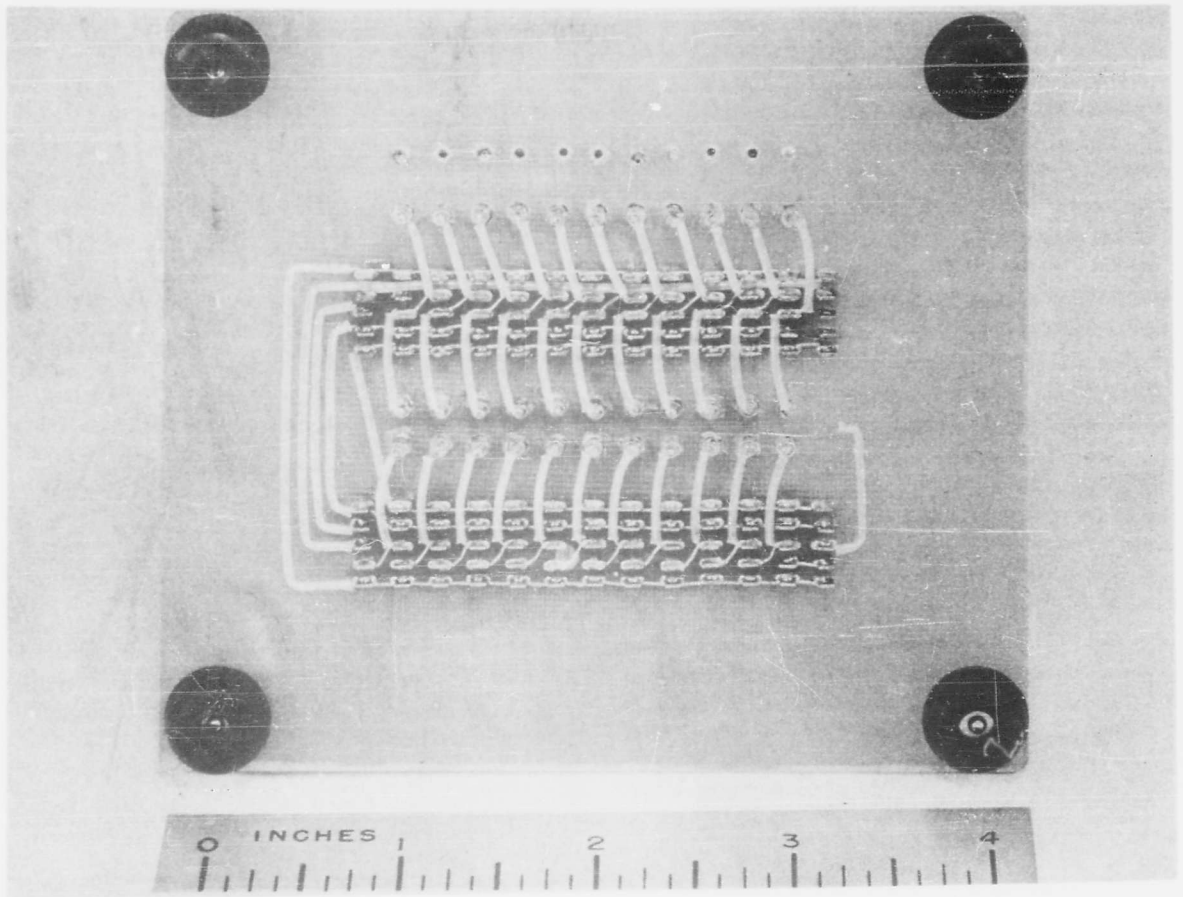
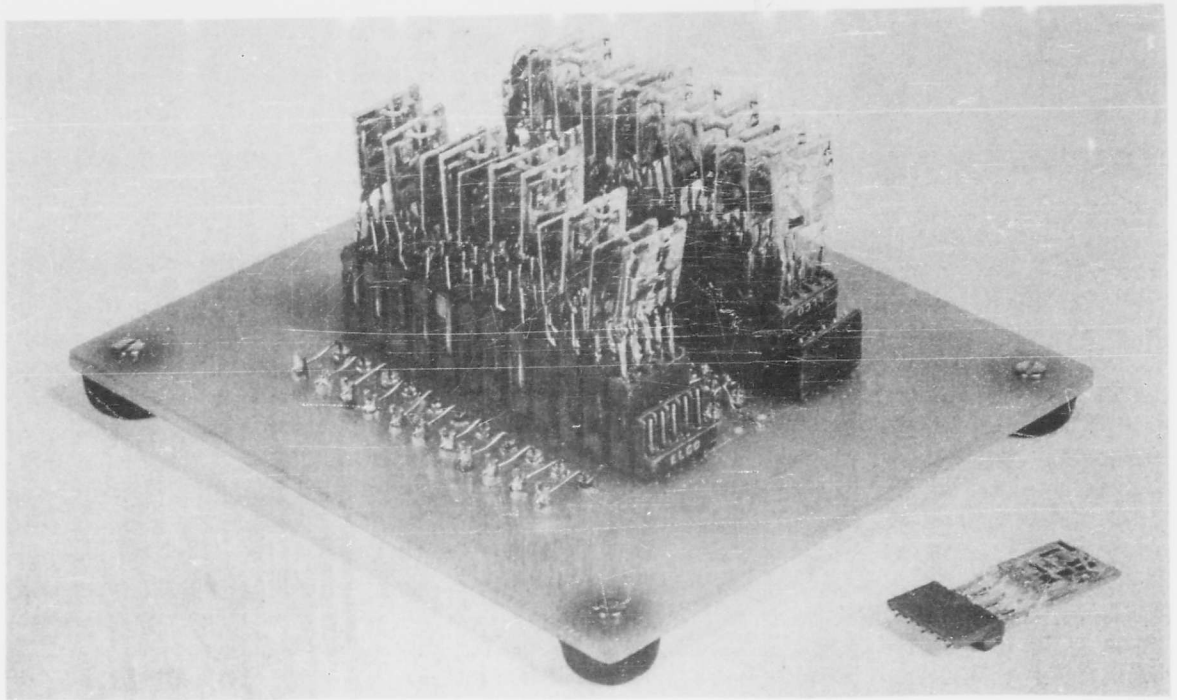


Figure 22. Portion of modified program timer breadboarded from 22 2D-binary dividers, 1 2D-NOR, 35 1N90 diodes and a few other miscellaneous conventional parts.



in the binary divider waveform at the point it was observed by momentarily turning "on" what should remain an "off" transistor.

- (1) High  $I_{co}$
- (2) Low  $V_{bb}$
- (3) High diode capacitance
- (4) Low diode back-resistance
- (5) Large input capacitors
- (6) High frequency transistor requiring low "turn on" charge

A consideration of the fabrication techniques employed focuses attention on the item "high diode capacitance." As was noted earlier, half-transistors were employed as diodes and because of the larger, and hence more convenient, collector dot, the base-collector junction was used. Unfortunately this has a relatively high capacitance particularly when compared with a point contact diode, the item usually employed for conventional construction. A suggestion was made to the contractor to begin using the emitter-base diode, and in units delivered later the spike was found to be eliminated or significantly diminished.

The effects of temperature on the voltage, frequency, and loading endpoints for a typical 2D-binary divider are shown in figure 10. The shape of these curves can be explained at least to the first order by the transistor parameters  $\beta$  and  $I_{co}$  (fig. 11) and the capacitance of the substrate (fig. 12). The increase in  $\beta$  with temperature explains (1) the heavier loading allowable at high temperature (both decreased load resistance and increased load capacitance) and (2) the lower value of  $V_{cc \text{ min}}$  required at high temperature. The increase in  $I_{co}$  at high temperature explains (1) the increase in  $V_{bb \text{ min}}$  required with increased temperature and (2) the increase in  $V_{cc \text{ min}}$  at high temperature.

The change in the dielectric constant of the substrate and hence the change in capacitance of the input capacitors with temperature explains the maximum frequency curve. Lower capacitance at both low and high temperature is translated into a shorter time constant in the input circuit and hence the ability to handle higher-frequency input signals.

It should be noted that with standard voltages and loads applied, the 2D-binary dividers currently being manufactured by the Sprague Electric Co. operate from about  $-70^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ . Performance becomes marginal at the extremes of this range.

Deposited metal techniques for the interconnection of 2D wafer circuits into subassemblies (ref 3) are currently frustrated by two factors. One is the probable cracking or straining of encapsulated plates during chucking for machining the surface preparatory to depositing metal for the interconnections. Work must be performed to

see if either a resilient coating around individual wafers or a method of controlling the chucking forces will alleviate the situation. The second item frustrating future work with deposited metal interconnections is the low order reliability associated with the present initial prototype 2D-binary dividers. A failure rate encompassing 10 to 15 percent of all units makes the probability of constructing an operational nine-stage countdown unit almost nil. And of course, replacement of defective wafers in an encapsulated assembly is impossible.

The welded interconnection technique, therefore, holds more promise at this stage of development. The major difficulty associated with welded connections is in making many tiny welds in a small volume. At the 2D level it appears as if connections will require at least 75 percent of an equipment volume. The additional factor that during prototype production the ability to replace defective parts at the single wafer level is an economic must will further increase connection volume. It is important to note that despite all the volume loss indicated, 2D assemblies will still be more than an order of magnitude smaller than conventionally packaged transistorized equipment.

From the limited amount of environmental testing performed, two important factors are evident. First, the transistors in the two units that were stored at high temperature are undergoing a decrease in  $\beta$  with time. This decrease is evident from the higher values of  $V_{cc \min}$  and the lower values of  $R_{L \min}$  shown in table II for longer times of storage. It is questionable, however, whether this decrease in  $\beta$  shown for transistors mounted in ceramic wafers is any more rapid than for conventionally packaged transistors of the 2N412 type. Certainly it is true that both 2D units under test are satisfactorily performing binary division and have been after more than 7000 hr of high temperature storage. It is also true that of the twelve units hermetically sealed in glass envelopes not one unit failed because of semiconductor degradation. In fact only one unit of the twelve failed at all and that was definitely a mechanical failure. Secondly, it is quite obvious that an inherent unreliability seems present in the mechanical connection to the semiconductor devices which is achieved with conductive adhesive.

The breadboard timer pictured in figure 22 demonstrated that operating 2D equipments can be assembled from 2D circuit wafers.

#### 4. CONCLUSIONS AND RECOMMENDATIONS

1. Additional 2D units should be purchased (1) incorporating changes recommended as a result of the evaluation performed on the initial 200 units, and (2) to increase the number of 2D wafer types so as to permit construction of complete 2D equipments. This objective is being accomplished by means of a supplementary contract also with the Sprague Electric Co. (DA49-186-502-ORD-969).

2. A mechanical engineering group should be assigned the problem of investigating presently proposed interconnection schemes and coming up with workable techniques for the realization of 2D equipments. This discipline is needed to complement the backgrounds of present personnel in Microminiaturization Branch.

3. More extensive evaluation testing should be inaugurated so that when the "debugging" period is completed some sort of reliability information will be available to engineers considering 2D systems.

## 5. ACKNOWLEDGMENTS

The author wishes to acknowledge the valuable assistance of the following individuals who made important contributions to this program:

Miss Emma Lee Hebb for encapsulation and metal deposition activities relative to the deposited metal interconnection technique, Mr. Amiel Goodman for assistance and comments relative to the failure analysis of 2D-binary dividers, Mr. George Lucey, Jr. for design of the 2D count-down unit pictured in figure 16, and Mr. Philip Emile, Jr. for his explanation of the "spike" phenomenon.

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